

## Product Overview

The NIRSP31 series devices are triple-channel digital isolators with integrated isolated DC-DC converter. The isolated DC-DC converter provides stable output voltage and up to 400mW output power by closed-loop control and transformer on chip. The feedback PWM signal is sent to primary side by a digital isolator based on Novosense capacity isolation technology. The high integrated solution can help simplify system design, save PCB area and improve reliability. The NIRSP31 series devices support 3kVrms insulation 1min withstand voltage. The data rate of the NIRSP31 series devices are up to 20Mbps, and the common-mode transient immunity (CMTI) is up to  $\pm 50\text{kV}/\mu\text{s}$ .

The NIRSP31 series devices provide 5V to 5V, 5V to 3.3V, 3.3V to 3.3V conversion mode. The output voltage can be set by SEL pin.

## Key Features

- Power supply voltage:
  - VDD: 3V to 3.6V, 4.5V to 5.5V for NIRSP31V
  - 4.5V to 5.5V for NIRSP31
  - VDDL: 1.8V to 3.6V, 4.5V to 5.5V
- Output Support Current:
  - 80mA for 5V to 5V/3.3V
  - 45mA for 3.3V to 3.3V
- Over current and over temperature protection
- Date rate: DC to 20Mbps
- High CMTI:  $\pm 50\text{kV}/\mu\text{s}$
- Propagation delay:  $<75\text{ns}$
- Operation temperature:  $-40^{\circ}\text{C}\sim 125^{\circ}\text{C}$
- RoHS-compliant packages: LGA-18

## Applications

- Industrial Battery Management System
- Industrial automation system
- Isolated RS232, RS485, CAN
- General-purpose multichannel isolation

## Device Information

Part Number	Package	Body Size
NIRSP31-DLARR	LGA 18	4.00 × 5.00mm
NIRSP31V-DLARR	LGA 18	4.00 × 5.00mm

## Functional Block Diagrams

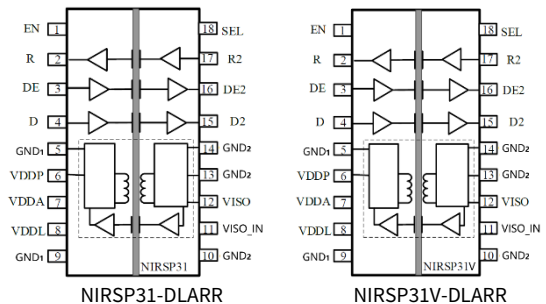


Figure 1. NIRSP31 Block Diagram

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## 1. Pin Configuration and Functions

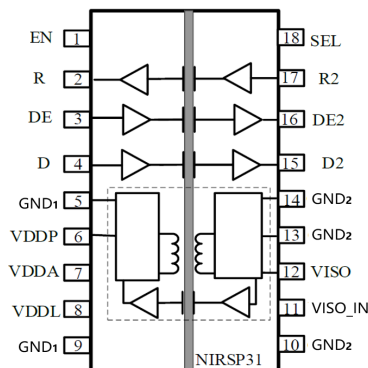


Figure 1.1 18-Pin LGA, Top View

Table1.1 Pin Functions

PIN NO.	SYMBOL	FUNCTION
1	EN	Power enable, When tied to VDDL or floating, the VISO output voltage is active. When a logic low voltage is applied, the VISO output voltage is shut down.
2	R	Logic Output of R2
3	DE	Logic Input of DE2
4	D	Logic Input of D2
5	GND <sub>1</sub>	Isolator Side 1 Ground, The ground reference for VDDP and VDDA.
6	VDDP	Power Supply for Isolator Side 1
7	VDDA	Analog Supply for Isolator Side 1, This pin must be connected VDDP.
8	VDDL	Side1 I/O logic Power Supply input
9	GND <sub>1</sub>	Isolator Side 1 Ground, The ground reference for VDDL.
10	GND <sub>2</sub>	Isolator Side 2 Ground, The ground reference for VISO_IN.
11	VISO_IN	Secondary Supply Voltage Input for Internal Load, this pin must be connected externally to VISO.
12	VISO	Secondary Supply Voltage Output Load
13	GND <sub>2</sub>	Isolator Side 2 Ground, The ground reference for VISO.
14	GND <sub>2</sub>	Isolator Side 2 Ground, The ground reference for VISO.
15	D2	Logic Output of D
16	DE2	Logic Output of DE
17	R2	Logic Input of R
18	SEL	VISO output voltage select, VISO=5V when SEL pulled up to VISO or floating; VISO=3.3V when SEL pulled low.

## 2. Device Comparison Table

The NIRSP31V devices provide 5V to 5V, 5V to 3.3V, 3.3V to 3.3V conversion modes. The NIRSP31 devices provide 5V to 5V, 5V to 3.3V conversion modes. The output voltage can be set by SEL pin, Supply configuration table is showed below.

VDDP	SEL PIN	NIRSP31V	NIRSP31
VDDP = (4.5V to 5.5V)	SEL = VISO	VISO = 5V	VISO = 5V
	SEL = GND <sub>2</sub>	VISO = 3.3V	VISO = 3.3V
VDDP = (3.0V to 3.6V)	SEL = GND <sub>2</sub>	VISO = 3.3V	/

## 3. Absolute Maximum Ratings

Parameters	Symbol	Min	Typ	Max	Unit
Power Supply Voltage	VDDP	-0.5		6.5	V
Maximum Input Voltage	DE, D	-0.4		VDDL+0.4	V
	R2	-0.4		VISO_IN+0.4	
Maximum Output Voltage	R	-0.4		VDDL +0.4	V
	DE2, D2	-0.4		VISO_IN+0.4	
Common-Mode Transients	CMTI	50			kV/us
Output current of digital channels	I <sub>o</sub>	-15		15	mA
Operating Temperature	T <sub>opr</sub>	-40		125	°C
Junction temperature	T <sub>J</sub>			150	°C
Storage Temperature	T <sub>stg</sub>	-65		150	°C
Electrostatic discharge	HBM			±2000	V
	CDM			±2000	V

## 4. Recommended Operating Conditions

Parameters	Symbol	min	typ	max	unit
Power Supply Voltage of NIRSP31V	VDDP、VDDA	3.0	3.3/5	5.5	V
Power Supply Voltage of NIRSP31	VDDP、VDDA	4.5	5	5.5	V
Power of VDDL	VDDL	1.8		5.5	V
Operating Temperature	T <sub>opr</sub>	-40		125	°C
High Level Input Voltage	V <sub>IH</sub>	0.7*VCC <sup>1</sup>		VCC	V
Low Level Input Voltage	V <sub>IL</sub>	0		0.3*VCC <sup>1</sup>	V
Data rate	DR			20	Mbps

(1) VCC of DE、D is VDDL; VCC of R2 is VISO\_IN.

## 5. Thermal Information

<i>Parameters</i>	<i>Symbol</i>	<i>LGA18</i>	<i>Unit</i>
IC Junction-to-Air Thermal Resistance	$\theta_{JA}$	72.4	°C/W
Junction-to-board thermal resistance	$\theta_{JB}$	33.8	°C/W
Junction-to-top characterization parameter	$\Psi_{JT}$	5.1	°C/W

### Notes

- (1) Four layers 2s2p PCB JEDEC JESD 51-7.
- (2) TX, RX and transformer loss distribution in line with the normal use of customers, and through simulation to obtain the thermal resistance parameters.

## 6. Specifications

### 6.1. Isolated DC/DC Converter Static Specifications

(VDDP=VDDA=4.5V~5.5V, SEL=VISO, Ta= -40°C to 125°C. Unless otherwise noted, Typical values are at VDDP=VDDA=5V, Ta=25°C, for NIRSP31 and NIRSP31V)

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Isolated Supply Voltage	VISO	4.5	5	5.5	V	
Line Regulation	VISO(LINE)			2	mV/V	I <sub>ISO</sub> = 40mA, VDDP=VDDA=4.5V to 5.5V
Load Regulation	VISO(LOAD)		0.4	5	%	I <sub>ISO</sub> = 8mA to 72 mA
Output Ripple	VISO(RIP)		64		mVpp	20-MHz bandwidth, I <sub>ISO</sub> = 40 mA, C <sub>LOAD</sub> = 0.1 μF    10 μF
Efficiency at maximum load current	EFF		50.6		%	I <sub>ISO</sub> = 80 mA, C <sub>LOAD</sub> = 0.1 μF    10μF
Output supply current	I <sub>ISO</sub>		80		mA	Ta= -40°C to 125°C
VDD supply current without digital isolator	I <sub>VDD_POWER</sub>		13		mA	No VISO Load
			157		mA	Full VISO Load(I <sub>ISO</sub> = 80mA)
Thermal Shutdown Temperature	T <sub>TSD</sub>		165		°C	
VDD supply current when EN is low	I <sub>VDD_POWER</sub>			30	μA	EN = 0, DE=GND <sub>1</sub> or VDDP, D= GND <sub>1</sub> or VDDP

(VDDP=VDDA=4.5V~5.5V, SEL=GND<sub>2</sub>, Ta=-40°C to 125°C. Unless otherwise noted, Typical values are at VDDP=VDDA=5V, Ta=25°C, for NIRSP31 and NIRSP31V)

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Isolated Supply Voltage	VISO	3	3.3	3.6	V	
Line Regulation	VISO(LINE)			6	mV/V	I <sub>ISO</sub> = 40mA, VDDP=VDDA=4.5V to 5.5V
Load Regulation	VISO(LOAD)		0.6	5	%	I <sub>ISO</sub> = 8mA to 72 mA
Output Ripple	VISO(RIP)		57.7		mVpp	20-MHz bandwidth, I <sub>ISO</sub> = 40 mA, C <sub>LOAD</sub> = 0.1 μF    10 μF
Efficiency at maximum load current	EFF		40.8		%	I <sub>ISO</sub> = 80 mA, C <sub>LOAD</sub> = 0.1 μF    10μF
Output supply current	I <sub>ISO</sub>		80		mA	Ta= -40°C to 125°C
VDD supply current without digital isolator	I <sub>VDD_POWER</sub>		11		mA	No VISO Load
			129		mA	Full VISO Load(I <sub>ISO</sub> =80mA)

(VDDP=VDDA=4.5V~5.5V, SEL=GND<sub>2</sub>, Ta=-40°C to 125°C. Unless otherwise noted, Typical values are at VDDP=VDDA=5V, Ta=25°C, for NIRSP31 and NIRSP31V)

Thermal Shutdown Temperature			165		°C	
VDD supply current when EN is low	I <sub>VDD_POWER</sub>			27	µA	EN = 0, DE=GND <sub>1</sub> or VDDP, D= GND <sub>1</sub> or VDDP

(VDDP=VDDA=3.0V~3.6V, SEL=GND<sub>2</sub>, Ta=-40°C to 125°C. Unless otherwise noted, Typical values are at VDDP=VDDA=3.3V, Ta=25°C, for NIRSP31V)

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Isolated Supply Voltage	VISO	3	3.3	3.6	V	
Line Regulation	VISO(LINE)			2	mV/V	I <sub>ISO</sub> = 40mA, VDDP=VDDA=3.0V to 3.3V
Load Regulation	VISO(LOAD)		0.6	5	%	I <sub>ISO</sub> = 4.5mA to 40.5 mA
Output Ripple	VISO(RIP)		48.9		mVpp	20-MHz bandwidth, I <sub>ISO</sub> = 40 mA, C <sub>LOAD</sub> = 0.1 µF    10 µF
Efficiency at maximum load current	EFF		40.9		%	I <sub>ISO</sub> = 45 mA, C <sub>LOAD</sub> = 0.1 µF    10µF
Output supply current	I <sub>ISO</sub>		45		mA	(Ta= -40°C to 125°C)
VDD supply current without digital isolator	I <sub>VDD_POWER</sub>		11		mA	No VISO Load
			110		mA	Full VISO Load(I <sub>ISO</sub> =45mA)
Thermal Shutdown Temperature			165		°C	
VDD supply current when EN is low	I <sub>VDD_POWER</sub>			24	µA	EN = 0, DE=GND <sub>1</sub> or VDDP, D= GND <sub>1</sub> or VDDP

## 6.2. Digital Isolator Electrical Characteristics

(VDDP=VDDA=4.5V~5.5V, SEL=VISO; VDDP=VDDA=4.5V~5.5V, SEL= GND<sub>2</sub>; VDDP=VDDA=3.0V~3.6V, SEL= GND<sub>2</sub>; Ta=-40°C to 125°C. Unless otherwise noted, Typical values are at VDDP=VDDA=5V, Ta=25°C)

Parameters	Symbol	Min	Typ	Max	Unit	Comments
High Level Input Voltage	V <sub>IH</sub>	0.7*VDDL			V	DE、 D
		0.7*VISO_IN				R2
Low Level Input Voltage	V <sub>IL</sub>			0.3*VDDL	V	DE、 D
				0.3*VISO_IN		R2
High Level Output Voltage	V <sub>OH</sub>	0.8*VDDL			V	R, I <sub>OH</sub> ≥ -4mA
		0.8*VISO_IN				DE2、 D2, I <sub>OH</sub> ≥ -4mA

(VDDP=VDDA=4.5V~5.5V, SEL=VISO; VDDP=VDDA=4.5V~5.5V, SEL= GND<sub>2</sub>; VDDP=VDDA=3.0V~3.6V, SEL= GND<sub>2</sub>; Ta=-40°C to 125°C. Unless otherwise noted, Typical values are at VDDP=VDDA=5V, Ta=25°C)

Low Level Output Voltage	V <sub>OL</sub>			0.2*VDDL	V	R, I <sub>OL</sub> ≤ 4mA
				0.2*VISO		DE2、D2, I <sub>OL</sub> ≤ 4mA
Output Impedance	R <sub>out</sub>		50		ohm	
High level input current	I <sub>IH</sub>		8	25	μA	DE =V <sub>DDL</sub>
low level input current	I <sub>IL</sub>	-25	-8		μA	EN、D、R2、SEL=0
EN logic high	V <sub>EN_H</sub>	0.7 *VDDL		VDDL	V	
EN logic low	V <sub>EN_L</sub>			0.3*VDDL	V	
Common Mode Transient Immunity	CMTI	50			kV/us	See <a href="#">Figure 6.6</a>

(VDDP=VDDA=4.5V~5.5V, SEL=VISO, Ta=-40°C to 125°C. Unless otherwise noted, Typical values are at VDDP=VDDA=5V, Ta=25°C, for NIRSP31 and NIRSP31V)

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Supply Current	IDD(Q0)		19		mA	All Input at 0V
	IDD(Q1)		14		mA	All Input at VCC <sup>1</sup>
	IDD(1M)		22		mA	All Input with square wave of 1Mbps, C <sub>L</sub> =15pF
Data Rate	DR	0		20	Mbps	
Minimum Pulse Width	PW			50	ns	Guaranteed by Design
Propagation Delay	t <sub>PLH</sub>		36	75	ns	See <a href="#">Figure 6.5</a> , C <sub>L</sub> = 15pF
	t <sub>PHL</sub>		36	75	ns	See <a href="#">Figure 6.5</a> , C <sub>L</sub> = 15pF
Pulse Width Distortion	PWD		5.0		ns	See <a href="#">Figure 6.5</a> , C <sub>L</sub> = 15pF
Rising Time	t <sub>r</sub>			5.0	ns	See <a href="#">Figure 6.5</a> , C <sub>L</sub> = 15pF
Falling Time	t <sub>f</sub>			5.0	ns	See <a href="#">Figure 6.5</a> , C <sub>L</sub> = 15pF
Channel-to-Channel Delay Skew	t <sub>sk(c2c)</sub>		8.0		ns	
Part-to-Part Delay Skew	t <sub>sk(p2p)</sub>		8.0		ns	

(1) VCC of DE、D is VDDL, VCC of R2 is VISO\_IN.



(VDDP=VDDA=4.5V~5.5V, SEL=GND<sub>2</sub>, Ta=-40°C to 125°C, Unless otherwise noted, Typical values are at VDDP=VDDA=5V, Ta=25°C, for NIRSP31 and NIRSP31V)

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Supply Current	IDD(Q0)		15		mA	All Input at 0V
	IDD(Q1)		13		mA	All Input at VCC <sup>1</sup>
	IDD(1M)		18		mA	All Input with square wave of 1Mbps, C <sub>L</sub> =15pF

(VDDP=VDDA=4.5V~5.5V, SEL=GND<sub>2</sub>, Ta=-40°C to 125°C. Unless otherwise noted, Typical values are at VDDP=VDDA=5V, Ta=25°C, for NIRSP31 and NIRSP31V)

Data Rate	DR	0		20	Mbps	
Minimum Pulse Width	PW			50	ns	Guarantee by Design
Propagation Delay	t <sub>PLH</sub>		36	75	ns	See <a href="#">Figure 6.5</a> , C <sub>L</sub> = 15pF
	t <sub>PHL</sub>		36	75	ns	See <a href="#">Figure 6.5</a> , C <sub>L</sub> = 15pF
Pulse Width Distortion	PWD		5.0		ns	See <a href="#">Figure 6.5</a> , C <sub>L</sub> = 15pF
Rising Time	t <sub>r</sub>			5.0	ns	See <a href="#">Figure 6.5</a> , C <sub>L</sub> = 15pF
Falling Time	t <sub>f</sub>			5.0	ns	See <a href="#">Figure 6.5</a> , C <sub>L</sub> = 15pF
Channel-to-Channel Delay Skew	t <sub>sk(c2c)</sub>		8.0		ns	
Part-to-Part Delay Skew	t <sub>sk(p2p)</sub>		8.0		ns	

(1) VCC of DE、D is VDDL; VCC of R2 is VISO.

(VDDP=VDDA=3.0V~3.6V, SEL=GND<sub>2</sub>, Ta=-40°C to 125°C. Unless otherwise noted, Typical values are at VDDP=VDDA=3.3V, Ta=25°C, for NIRSP31V)

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Supply Current	IDD(Q0)		15		mA	All Input at 0V
	IDD(Q1)		12		mA	All Input at VCC <sup>1</sup>
	IDD(1M)		17		mA	All Input with square wave of 1Mbps, C <sub>L</sub> =15pF
Data Rate	DR	0		20	Mbps	
Minimum Pulse Width	PW			50	ns	Guaranteed by Design
Propagation Delay	t <sub>PLH</sub>		36	75	ns	See <a href="#">Figure 6.5</a> , C <sub>L</sub> = 15pF
	t <sub>PHL</sub>		36	75	ns	See <a href="#">Figure 6.5</a> , C <sub>L</sub> = 15pF
Pulse Width Distortion	PWD		5.0		ns	See <a href="#">Figure 6.5</a> , C <sub>L</sub> = 15pF
Rising Time	t <sub>r</sub>			5.0	ns	See <a href="#">Figure 6.5</a> , C <sub>L</sub> = 15pF

(VDDP=VDDA=3.0V~3.6V, SEL=GND<sub>2</sub>, Ta=-40°C to 125°C. Unless otherwise noted, Typical values are at VDDP=VDDA=3.3V, Ta=25°C, for NIRSP31V)

Falling Time	t <sub>f</sub>			5.0	ns	See <a href="#">Figure 6.5</a> , C <sub>L</sub> = 15pF
Channel-to-Channel Delay Skew	t <sub>sk(c2c)</sub>		8.0		ns	
Part-to-Part Delay Skew	t <sub>sk(p2p)</sub>		8.0		ns	

(1) VCC of DE、D is VDDL; VCC of R2 is VISO.

### 6.3. Typical Performance Characteristics

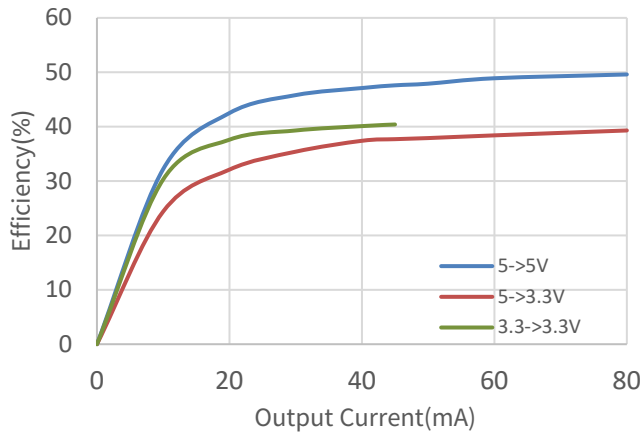


Figure 6.1 Output current vs efficiency

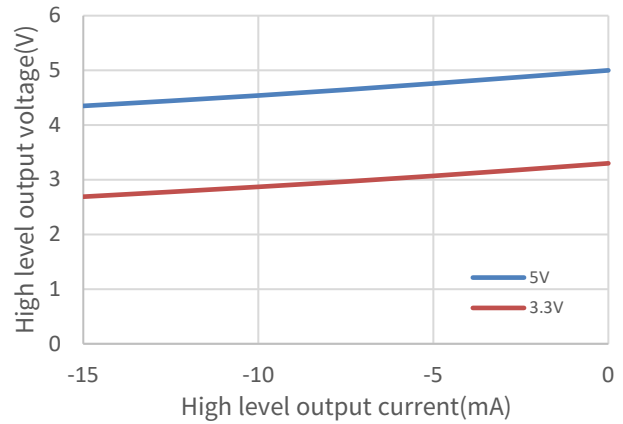


Figure 6.2 High-Level Output Voltage vs Output Current

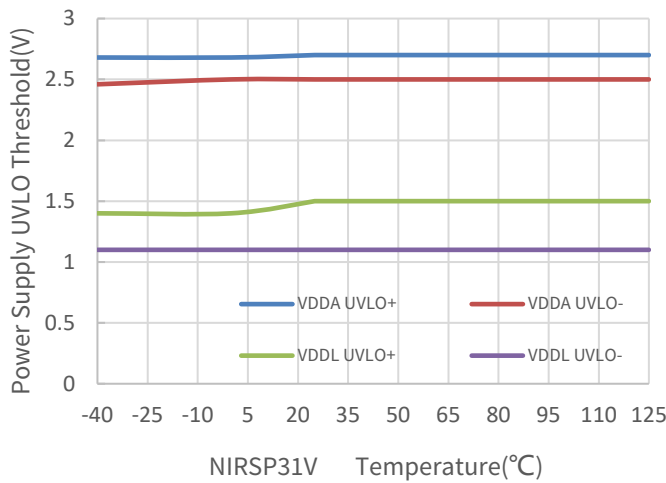


Figure 6.3 Power-Supply Undervoltage Threshold vs Temp

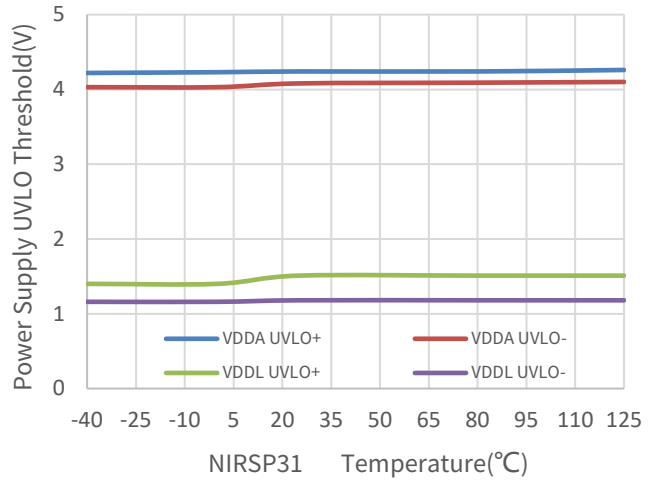


Figure 6.4 Power-Supply Undervoltage Threshold vs Temp

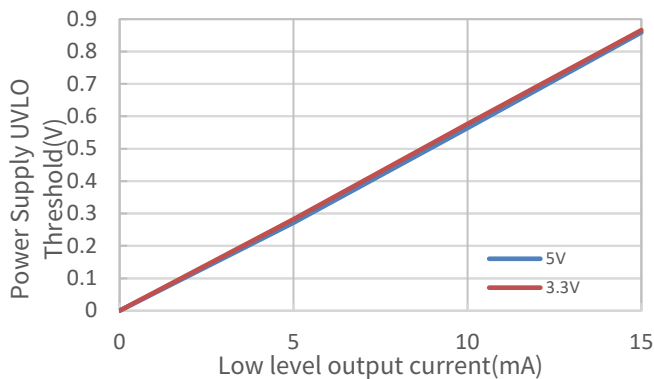


Figure 6.5 Low-Level Output Voltage vs Output Current

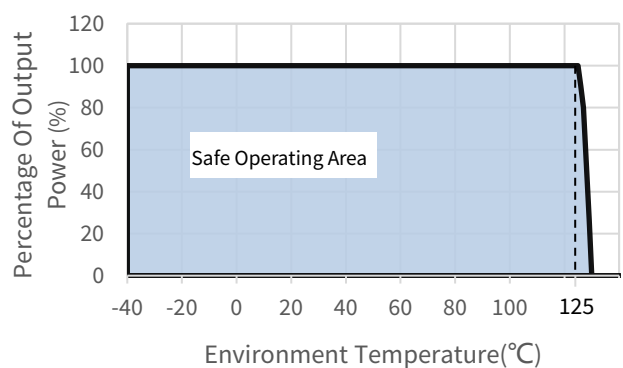


Figure 6.6 Temperature Derating Curve

6.4. Parameter Measurement Information

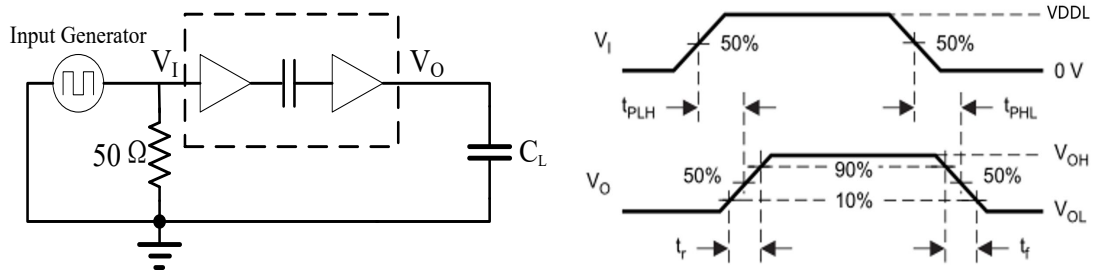


Figure 6.5 Switching Characteristics Test Circuit and Waveform

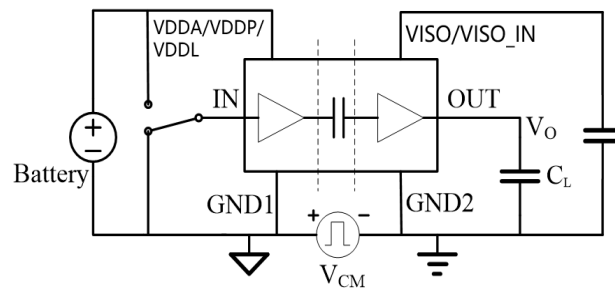


Figure 6.6 Common-Mode Transient Immunity Test Circuit

## 7. High Voltage Feature Description

Parameters	Symbol	value	unit	comments
Minimum External Air Gap (Clearance)	L(I01)	2.5	mm	Shortest terminal-to-terminal distance through air
Minimum External Tracking (Creepage)	L(I02)	2.5	mm	Shortest terminal-to-terminal distance across the package surface
Minimum Internal Gap	DTI	42.5	um	Distance through insulation
Maximum Isolation Voltage		3000	V <sub>RMS</sub>	t = 60 sec
Total Power Dissipation at 25°C	Ps	1726	mW	
Safety Input, Output, or Supply Current	Is	313.91	mA	$\theta_{JA} = 72.4^{\circ}\text{C}/\text{W}$ , $V_{DDP} = V_{DDA} = V_{DDL}$ $= V_{ISO\_IN} = 5.5\text{ V}$ , $T_J = 150^{\circ}\text{C}$ , $T_a = 25^{\circ}\text{C}$ .
Max Safety Temperature	Ts	150	°C	

## 8. Function Description

The NIRSP31 series devices are triple-channel digital isolators with integrated isolated DC-DC converter. The isolated DC-DC converter provide up to 400mW output power using on-chip transformer. The feedback PWM signal is sent to primary side by a digital isolator. The NIRSP31 series devices support 3kVrms insulation 1min withstand voltage. The data rate of the NIRSP31 is up to 20Mbps, and the common-mode transient immunity (CMTI) is up to 50kV/us. The logical level of digital isolators on left side can be set by VDDL pin, which can support the application when the supply voltage and I/O voltage level are different.

The high integrated solution can help to simplify system design and improve reliability. Because of its smaller package of LGA, the NIRSP31 series devices are suitable for the limited PCB space applications. Meanwhile, the devices are also suitable for wide temperature application, which most power modules cannot support.

### 8.1. Device Functional Modes

The NIRSP31 series devices provide triple-channel digital isolators. The digital isolators have default output status when VCCIN is unready and VCCOUT is ready as shown in below table.

VCCIN <sup>1</sup> status	VCCOUT status	Input			Output			Comment
		D	DE	R2	D2	DE2	R	
Ready <sup>2</sup>	Ready	H	H	H	H	H	H	Normal operation
Ready	Ready	L	L	L	L	L	L	
Ready	Ready	floating	floating	floating	H	L	H	
Unready	Ready	X	X	X	H	L	X	
Ready	Unready	X	X	X	X	X	H	

(1) VCCIN is VDDP, VDDA, VDDL and VCCOUT is VISO.

(2) Ready = Powered up; Unready = Powered down; X = Irrelevant; H = High level; L = Low level.

### 8.2. Output Short and Over Temperature Protection

The NIRSP31 series devices are protected against output short. When the devices detect the output is short, the device will be in Hiccup mode and the transferred power will be limited. So the temperature of the device will be low, and the device is protected. The NIRSP31 series devices are also protected against over temperature. When devices detect the chip is over 165°C, the chip will be shut down until the temperature of the device is below 145°C.

## 9. Application Note

### 9.1. Typical Application

The NIRSP31 requires 0.1 μF and 10uF bypass capacitors between VDDP&VDDA and GND<sub>1</sub>、 VISO and GND<sub>2</sub>, a 0.1uF bypass capacitor between VDDL and GND<sub>1</sub> , VISO\_IN and GND<sub>2</sub> . The capacitor should be placed as close as possible to the package. This is very important for the performance of the device. The Figure 9.1 is the typical isolated RS485 schematic using NIRSP31.

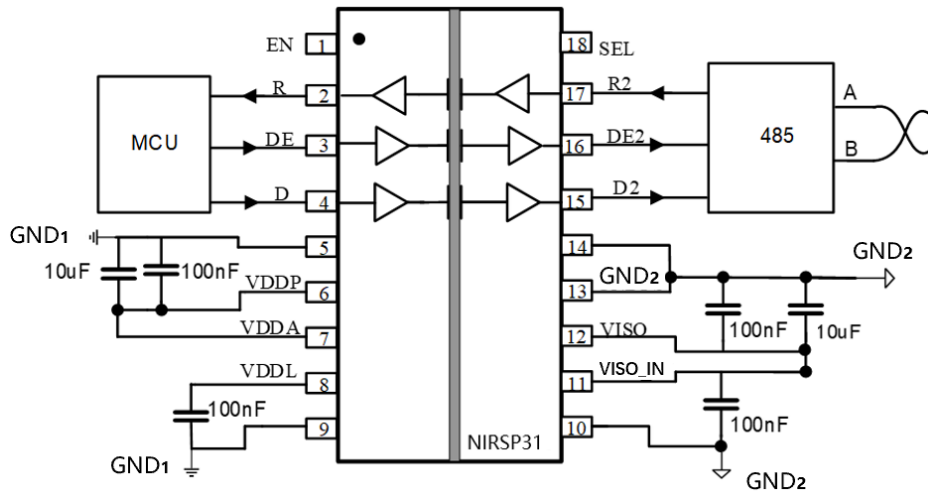


Figure 9.1 Isolated RS485 schematic using NIRSP31

### 9.2. PCB Layout

The low ESR capacitors should be connected between Pin 5 (GND<sub>1</sub>) and Pin 6 (VDDP), Pin 7 (VDDA), Pin 8(VDDL) and Pin 9 (GND<sub>1</sub>). The VISO\_IN capacitors are connected between Pin 10 (GND<sub>2</sub>) and Pin 11 (VISO\_IN), The VISO capacitors Pin 12 (VISO) and Pin13 (GND<sub>2</sub>). To suppress noise and reduce ripple, a parallel combination of at least two capacitors is required with the smaller of the two capacitors located closest to the device. The recommended capacitor values are 0.1 μF and 10 μF for VDDP between Pin 5 and Pin 6. Capacitor values of 0.1 μF are recommended for VISO\_IN between Pin 10 and Pin 11, for VDDL Pin 8 and Pin 9. The recommended best practice is to use a very low inductance ceramic capacitor, or its equivalent, for the smaller value capacitors. The total lead length between both ends of the capacitor and the input power supply pin should not exceed 10 mm.

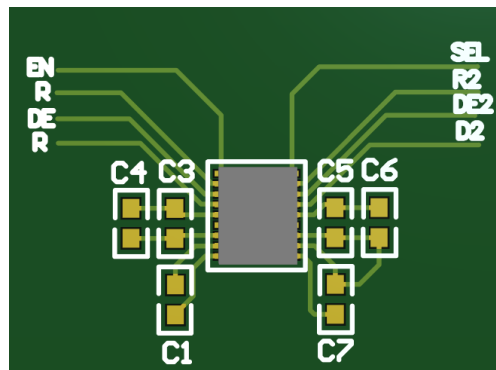
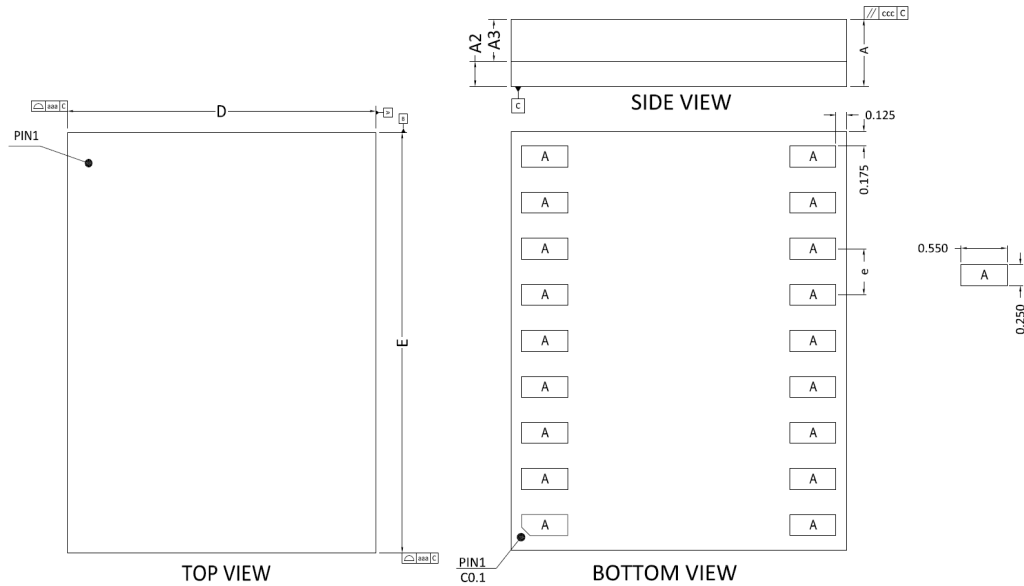


Figure 9.2 Recommended PCB Layout

### 10. Package Information



MILLIMETER			
SYMBOL	MIN	NOR	MAX
A	0.71	0.80	0.89
A2	0.26	0.30	0.34
A3	0.45	0.50	0.55
D	3.90	4.00	4.10
E	4.90	5.00	5.10
e	0.55 BSC		
aaa	0.10		
ccc	0.05		

Figure 10.1 LGA18 Package Shape and Dimension in millimeters

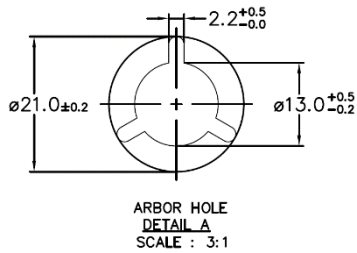
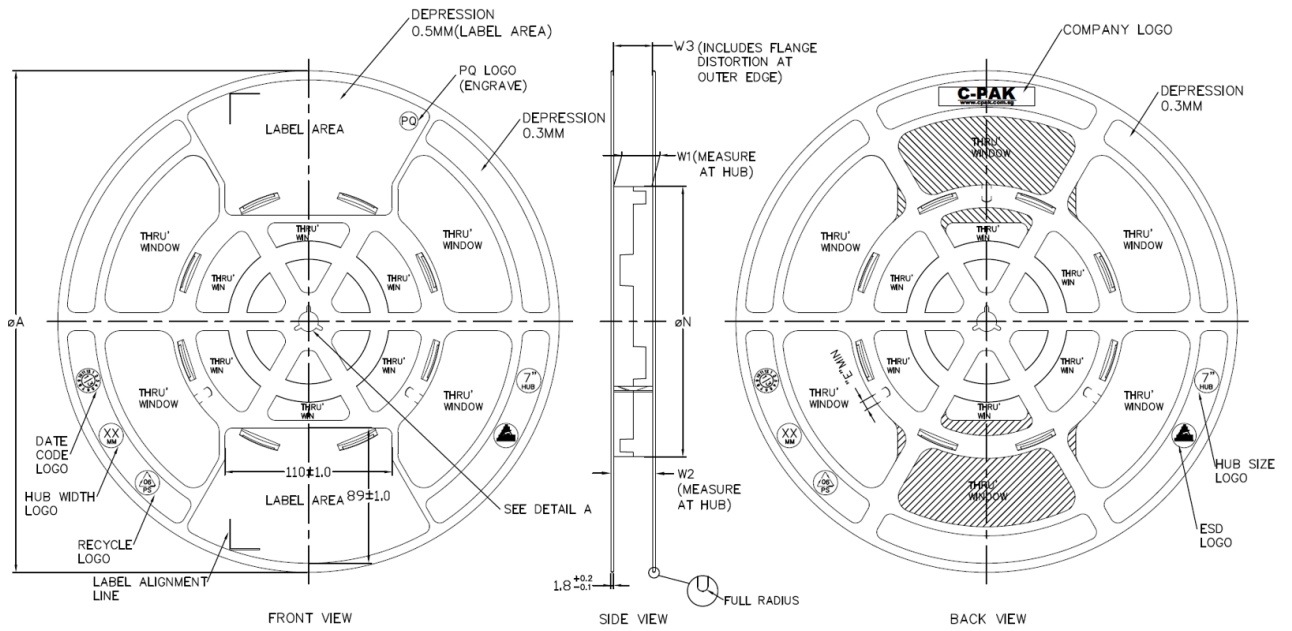
### 11. Order Information

Part Number	Isolation Rating (kV)	Number of side 1 inputs	Number of side 2 inputs	Max Data Rate (Mbps)	Temperature	MSL	Package Type	Package Drawing	SPQ
NIRSP31-DLARR	3	2	1	20	-40 to 125°C	3	LGA18	LGA18	3000
NIRSP31V-DLARR	3	2	1	20	-40 to 125°C	3	LGA18	LGA18	3000

### 12. Documentation Support

Part Number	Product Folder	Datasheet	Technical Documents	Isolator selection guide
NIRSP31	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>
NIRSP31V	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>

### 13. Tape and Reel Information



PRODUCT SPECIFICATION						
TAPE WIDTH	øA ±2.0	øN ±2.0	W1	W2 (MAX)	W3	E (MIN)
08MM	330	178	8.4 <sup>+0.8</sup> <sub>-0.8</sub>	14.4	SHALL ACCOMMODATE TAPE WIDTH WITHOUT INTERFERENCE	5.5
12MM	330	178	12.4 <sup>+2.0</sup> <sub>-2.0</sub>	18.4		5.5
16MM	330	178	16.4 <sup>+2.0</sup> <sub>-2.0</sub>	22.4		5.5
24MM	330	178	24.4 <sup>+2.0</sup> <sub>-2.0</sub>	30.4		5.5
32MM	330	178	32.4 <sup>+2.0</sup> <sub>-2.0</sub>	38.4		5.5

SURFACE RESISTIVITY			
LEGEND	SR RANGE	TYPE	COLOUR
A	BELOW 10 <sup>12</sup>	ANTISTATIC	ALL TYPES
B	10 <sup>9</sup> TO 10 <sup>11</sup>	STATIC DISSIPATIVE	BLACK ONLY
C	10 <sup>8</sup> & BELOW 10 <sup>8</sup>	CONDUCTIVE (GENERIC)	BLACK ONLY
E	10 <sup>9</sup> TO 10 <sup>11</sup>	ANTISTATIC (COATED)	ALL TYPES

Figure 13.1 Tape and Reel Information of LGA18



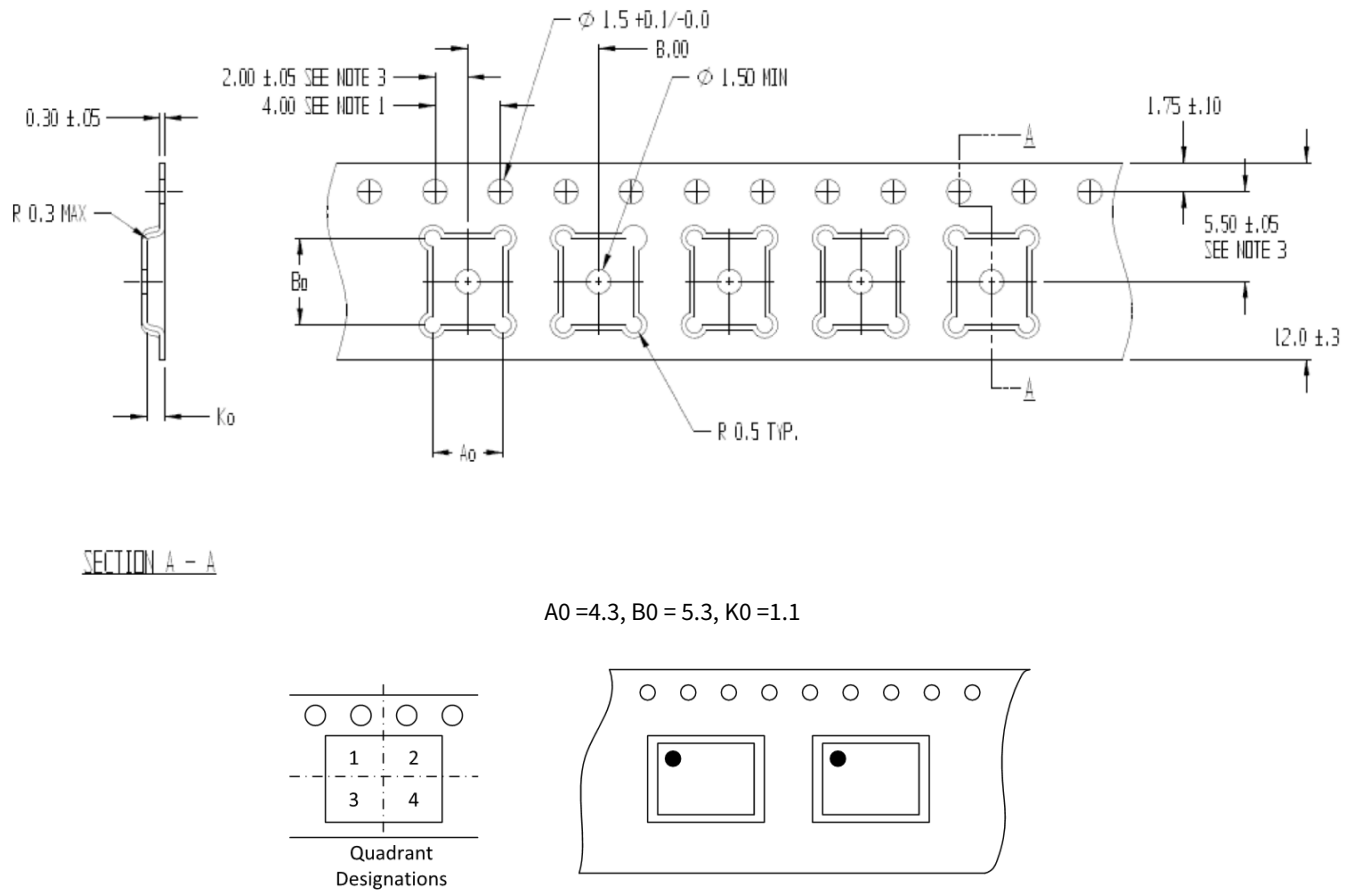


Figure 13.2 Tape and Reel Information of LGA18

## 14. Revision History

Revision	Description	Date
1.0	Initial Version	2022/12/25
1.1	1. Updated 3.3V to 3.3V output to support 45mA and related parameters; 2. Add safe operating area curve; 3. Updated output supply current 80mA min to typ(5V-5V/3.3V); 4. Deleted material group value; 5. Deleted figure 7.1 (Thermal Derating Curve for Safety Limiting Current per VDE); 6. Updated line regulation 2mV/V to 6mV/V for (5V-3.3V).	2023/4/12
1.2	1.Updated EN pin Power enable, when tied to VDDP or floating change to When tied to VDDL or floating; 2. Add VDDA and VDDL voltage working ranges; 3. Add EN Logic high and logic low threshold.	2023/5/26

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